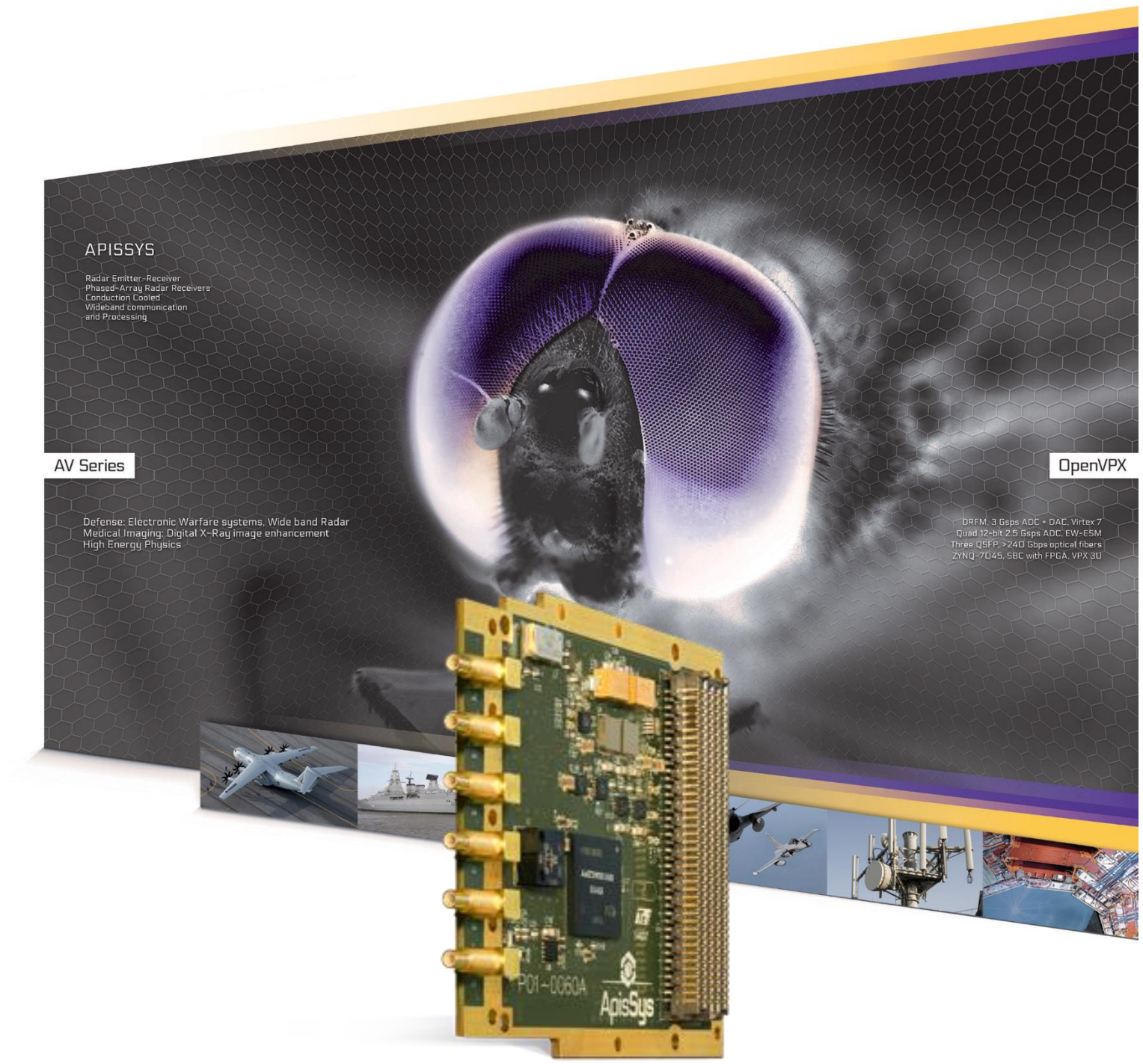


AF204

Arbitrary Broadband Signal Generation
L and S bands
Automatic Test Equipment (ATE)

FMC HPC

Single 12 bit 3 Gsps DAC

Conduction or Air-Cooled

ApisSys

High Speed Data Conversion
& Signal Processing Solutions

AF204

Applications

- Test and Measurement
- Radar Transmitter
- Software Defined Radio

Features

- 1 channel 12-bit, 3 Gsps DAC
- External clock and reference input
- Internal low jitter clock generation
- External trigger input and output
- VITA 57 FMC form factor
- Air cooled and Conduction cooled rugged versions
- FPGA firmware cores
- Windows® and Linux® drivers

Overview

The AF204 is part of ApisSys' range of modular IOs solutions based on the VITA 57, FPGA Mezzanine Card standard.
The AF204 provides customers with a single channel 12-bit up to 3 Gsps DAC capability, ideally suited for test and measurement, Software Defined Radio or Radar Transmitter applications.
The AF204 DAC channel is AC coupled with an output bandwidth wider than 5 GHz for a full scale signal of -2 dBm (500 mVpp).
The AF204 provides an internal ultra low jitter clock generation and can be used with either an external clock or an external reference for higher flexibility.
The AF204 features an external trigger input and an external trigger output used to synchronize processing with external events.
The AF204 is fully supported on ApisSys 3U VPX FPGA processing engines, making it ideally suited for test and measurement, Software Defined Radio or Ultra Wideband Radar Transmitters applications.

12-bit 3 Gsps Digital-Analog Converter

The AF204 Digital to Analog conversion is performed by one e2v EV12DS130 12-bit 3 Gsps DAC.

The AF204 provides one front panel SSMC connector for the analog output.

The output signal is single ended AC coupled with an output bandwidth from 1 MHz to more than 5 GHz with -2 dBm output level.

Clock

The AF204 provides an internal ultra low jitter clock generator locked on a 100 MHz internal reference.

The AF204 provides a front panel SSMC connector for an external reference from 10 to 100 MHz, a front panel SSMC connector for an external clock input from 500 MHz to 3 GHz and a front panel SSMC connector for an external clock output.

Estimated jitter from the internal clock generation (including 100 MHz reference and clock distribution) is below 200 fs for a 3 GHz clock. Added jitter on external clock is lower than 100 fs.

Trigger and Synchronization

The AF204 provides a front panel SSMC connector for an external trigger input and one front panel SSMC connector for an external trigger output.

The trigger input and output signals are buffered with ultrafast PECL buffers.

FMC interface

The AF204 features a VITA 57 – FMC (FPGA Mezzanine Card) compliant slot.

The FMC uses High Pin Count (HPC) interface with 1.8V or 2.5V Vadj.

The FMC MGT interfaces are unused.

Firmware

The AF204 comes with a firmware package which includes VHDL cores allowing control and communication with all AF204 hardware resources.

A base design is provided which demonstrates the use of the AF204 and gives users a starting point for firmware development.

The AF204 firmware package is supported on the Xilinx ISE® 14 design suite.

The AF204 firmware package has been fully validated on AV103 and other ApisSys FMC carrier products.

Software

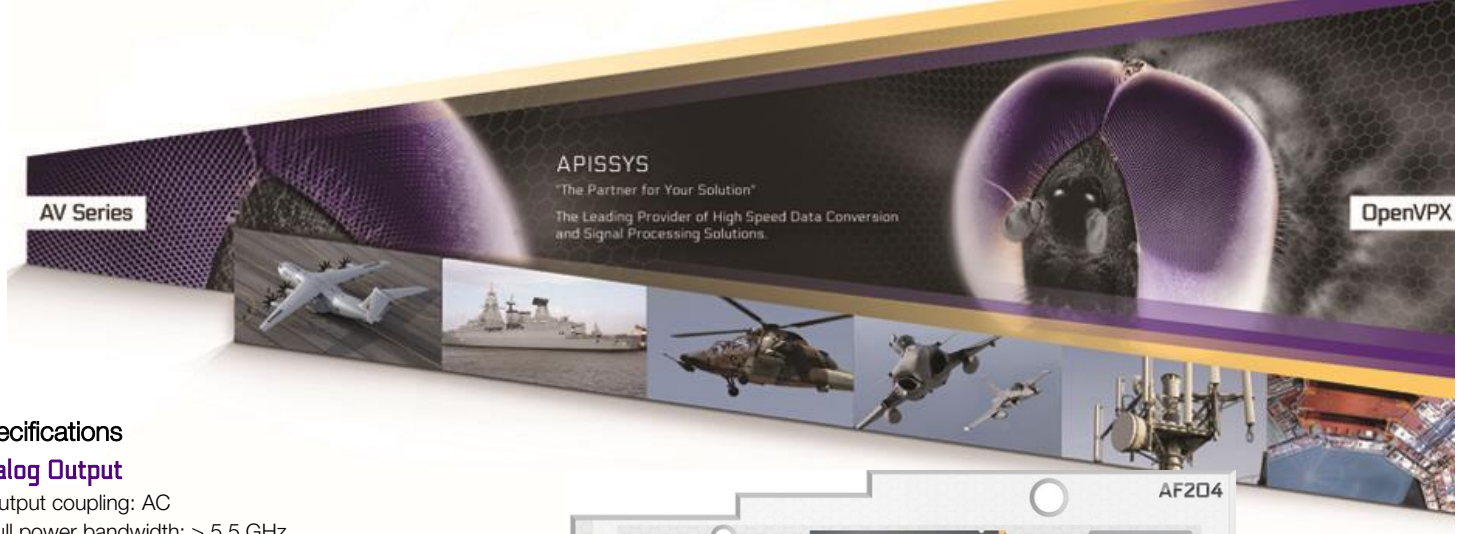
The AF204 is delivered with control software for Windows XP and 7, and Linux, compatible with AV103 and other ApisSys FMC carrier products.

An application example is provided as source code.

Ruggedization

The AF204 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6 and ECC3.



Specifications

Analog Output

- Output coupling: AC
- Full power bandwidth: > 5.5 GHz
- Full scale : -2 dBm
- Impedance: 50 Ohms
- Connector: SSMC

Digital - Analog Conversion

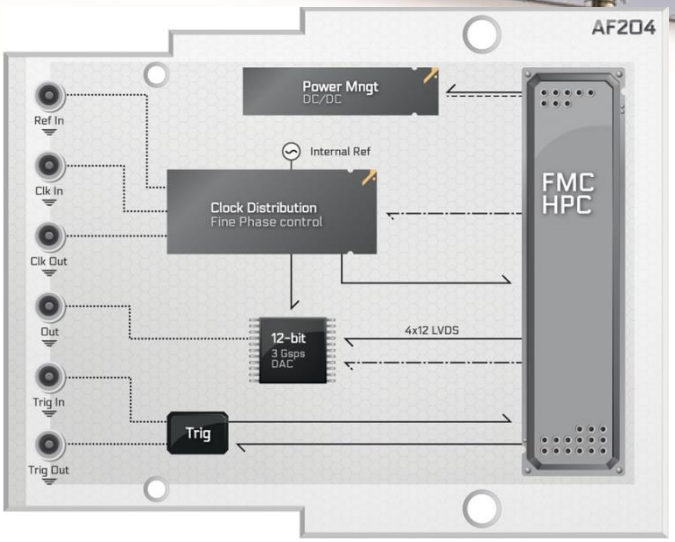
- Single channel
- Resolution: 12 bit
- Sampling Frequency 500MHz to 3.0 GHz

Sampling Performances

- 3 Gsps, Fout: 800 MHz, -1dBFS, NRZ:
  - SFDR: 66 dBc
  - Clock spur: -77 dBc (Fc/2)
- 3 Gsps, Fout: 1.6 GHz, -1dBFS, RF:
  - Noise Density: -154 dBm/Hz
  - SFDR: 52 dBc
  - Clock spur: -84 dBc (Fc/2)
  - Clock spur: -41 dBc (Fc)
- 3 Gsps, Fout: 3.8 GHz, -1dBFS, RF:
  - Noise Density: -139 dBm/Hz
  - SFDR: 52 dBc

Clock

- Internal low jitter clock:
  - 500 MHz to 3 GHz GHz
  - Internal jitter: < 200 fs
- External Input Clock:
  - frequency: 500 MHz to 3 GHz
  - Level: 10 dBm to 15 dBm
  - Added jitter (Ext clock) < 100 fs
  - Connector: SSMC, 50 Ohms
- External Output Clock:
  - frequency: sampling clock
  - Level: 0 dBm
  - Connector: SSMC, 50 Ohms
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Level: 10 dBm to 15 dBm
  - Connector: SSMC, 50 Ohms



Trigger

- External trigger Input
  - External Input: 0V to 2Vp
  - Connector: SSMC, 50 Ohms
- External Trigger Output
  - External Input: 0V to 2Vp
  - Connector: SSMC

FMC interface

- HPC:
  - LA(0:33): LVDS 1.8V or 2.5V
  - HA(0:23): LVDS 1.8V or 2.5V
  - HB(0:21): LVCMOS 1.8V or 2.5V

Software support

- Software Drivers:
  - Windows 7
  - Linux
- Application example:
  - Windows and Linux

Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx ISE 14

Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3

Power dissipation

- +12V: 0.5 A max (6.1W)
- VADJ (1.8V or 2.5V): 0.2 A max (0.4W)
- +3.3V: 0.2 A max (0.7W)
- +3.3VAUX: 0.1 A max (0.4W)

Weight

- Air cooled : 50g
- Conduction cooled : 55g

Ordering information

Part Number		AF204	–	rr
Ruggedization level	Air Standard		-	AS
	Air Rugged		-	AR
	Conduction Standard		-	CS

Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.1 g^2/Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 30,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (default acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

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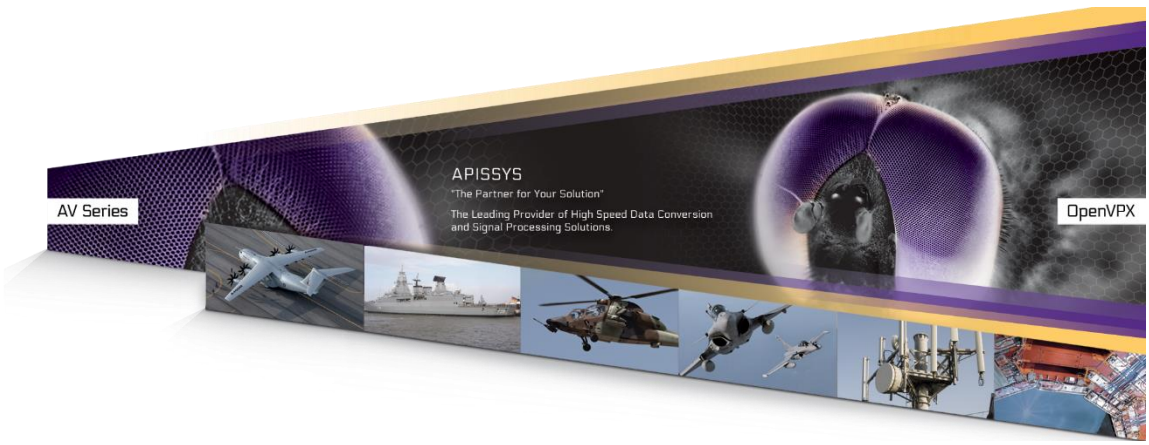

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